Summary

Data processing units with a circuit configuration for connecting a first communication bus with a second communication bus

The present invention relates to a data processing configuration with a first circuit configuration (1) that connects a communication bus (2) with a second communication bus (3). The first circuit configuration (1) is the bus master of the first communication bus (2). Furthermore, a second circuit configuration (4) is connected with the first communication bus (2). By employing a wait signal (11), which is generated in the second circuit configuration (4) and transmitted to the first circuit configuration (1), it is possible to expand read and write access to the first communication bus (2) to any random number of clock cycles.

Figure 1